REMARKS

The Examiner objected to the Specification for failing to provide proper antecedent basis for the claimed subject matter. In particular, the Examiner stated that claims 32 – 34 and 39 – 41 recite that the act of "detecting the presence of the switch" in claims 32 and 39, the act of "determining the number of primary ports present in the switch" in claims 33 and 40, and the act of "storing the value" in claims 34 and 41 include "issuing a configuration transaction." The Examiner then states that the "specification fails to provide proper basis for the claimed limitations."

Support for "detecting the presence of the switch" by "issuing a configuration transaction" as recited in claims 32 and 39 can be found, for example, on page 12, lines 6 – 18, which is reproduced below.

> "Next, the software probes the first HT I/O interconnect 540 to determine if any HT I/O devices are coupled to the bus.
>
> 5.6.1 Type0 Configuration Transactions
>
> One method of probing the HT I/O interconnect 540 is issuing a type0 configuration read transaction from the host processor 505 onto the HT I/O interconnect 540. Type0 configuration read transactions retrieve information from configuration registers that are located within HT I/O devices that are coupled to an HT I/O interconnect and return such information to the issuer of the transaction. Similarly, a type0 configuration write transaction stores information in the configuration registers that are located within HT I/O devices that are coupled to an HT I/O interconnect.
>
> When the host processor 505 issues a type0 configuration read transaction on the HT I/O interconnect 540, the capabilities of the first HT switch 510 can be retrieved."

Support for "determining the number of primary ports present in the switch" by "issuing a configuration transaction" as recited in claims 33 and 40 is present in the Specification. For example, such support can be found on page 12, lines 17 – 21 of the Specification, which is reproduced below.

> "When the host processor 505 issues a type0 configuration read transaction on the HT I/O interconnect 540, the capabilities of the first HT switch 510 can be retrieved. Because the retrieved capabilities would indicate that an HT switch is coupled to I/O bus 540, the host processor 505 would issue one or more type0 read transactions that retrieve the number of ports in the first HT switch 510."

Support for "storing the value" by "issuing a configuration transaction" as recited in claims 34 and 41 can be found, for example, on page 12, lines 14 – 16, which is reproduced below.

> "Similarly, a type0 configuration write transaction stores information in the configuration registers that are located within HT I/O devices that are coupled to an HT I/O interconnect."

Thus, Applicant believes that the Specification provides proper basis for the claimed limitations.

The Examiner objected to claim 15 for failing to further limit the subject matter of a previous claim. As a result, Applicant has canceled claim 15.

The Examiner objected to claim 47 as being a substantial duplicate of claim 44. Applicant submits that claims 44 and 47 claim two distinct embodiments of Applicant's invention. As a result, Applicant has canceled claim 47.

The Examiner rejected claims 32 – 34 and 39 - 41 under 35 U.S.C. § 112, first paragraph because the Specification "while being enabling for issuing a configuration transaction (See Application, pages 2 – 4), does not reasonably provide enablement for issuing a configuration transaction included in the method steps of detecting the presence of the switch (See Claims 32 and 39), determining the number of primary ports present in the switch (See Claims 33 and 40), and/or storing the value (See Claims 34 and 41). . . . The Examiner doubts how the steps of detecting the presence of the switch, determining the number of primary ports present in the switch, and/or storing the value could include the method step of issuing a configuration transaction in light of the specification."

As discussed above, (a) detecting the presence of a switch, (b) determining the number of primary ports in a switch, and (c) storing values by issuing configuration transactions are fully disclosed in the Specification. For example, such acts are disclosed in the Specification on page 12, lines 6 – 16, which are reproduced below.

> "Next, the software probes the first HT I/O interconnect 540 to determine if any HT I/O devices are coupled to the bus.
>
> 5.6.1 Type0 Configuration Transactions
>
> One method of probing the HT I/O interconnect 540 is issuing a type0 configuration read transaction from the host processor 505 onto the HT I/O

interconnect 540. Type0 configuration read transactions retrieve information from configuration registers that are located within HT I/O devices that are coupled to an HT I/O interconnect and return such information to the issuer of the transaction. Similarly, a type0 configuration write transaction stores information in the configuration registers that are located within HT I/O devices that are coupled to an HT I/O interconnect."

Thus, Applicant believes that Claims 32 – 34 and 39 – 41 fully comply with 35 U.S.C. § 112, first paragraph.

The Examiner rejected claims 7 and 22 under 35 U.S.C. § 112, second paragraph for insufficient antecedent basis for the limitation "the first configuration." Applicant has amended claims 7 and 22 to clarify the antecedent basis.

The Examiner rejected claim 30 under 35 U.S.C. § 112, second paragraph for insufficient antecedent basis for the limitation "the primary segment number." Applicant has amended claim 30 to clarify the antecedent basis.

The Examiner rejected claims 35 and 42 under 35 U.S.C. § 112, second paragraph for insufficient antecedent basis for the limitation "the span of the highest numbered segment." Applicant has amended claims 35 and 42 to clarify the antecedent basis.

The Examiner rejected claim 37 under 35 U.S.C. § 112, second paragraph for insufficient antecedent basis for the limitation "the secondary segment number." Applicant has amended claim 37 to clarify the antecedent basis.

The Examiner rejected claims 1 and 15 under 35 U.S.C. § 102(b) as being anticipated by PCI-to-PCI Bridge Architecture Specification ("PCI-to-PCI Bridge"). As discussed above, Applicant has canceled claim 15.

In order to clearly distinguish claim 1 from the cited prior art, the Applicant has amended claim 1 to expressly require that the claimed first and second switches be HyperTransport ("HT") switches. Thus, none of the prior art cited by the Examiner, alone or in any combination, performs the method claimed in amended claim 1. As a result, Applicant believes that independent claim 1, together with dependent claims 2 - 14 are allowable.

The Examiner rejected claim 16 under 35 U.S.C. § 102(b) as being anticipated by PCI-to-PCI Bridge Architecture Specification ("PCI-to-PCI Bridge"). In order to clearly distinguish claim 16 from the cited prior art, the Applicant has amended claim 16 to expressly require that

the claimed first and second switches be HyperTransport ("HT") switches. Thus, none of the prior art cited by the Examiner, alone or in any combination, performs the method claimed in amended claim 16. As a result, Applicant believes that independent claim 16, together with dependent claims 17 – 28 are allowable.

The Examiner rejected claim 29 under 35 U.S.C. § 102(b) as being anticipated by PCI-to-PCI Bridge Architecture Specification ("PCI-to-PCI Bridge"). In order to clearly distinguish claim 29 from the cited prior art, the Applicant has amended claim 29 to expressly require that the claimed switch be a HyperTransport ("HT") switch. Thus, none of the prior art cited by the Examiner, alone or in any combination, performs the method claimed in amended claim 29. As a result, Applicant believes that independent claim 29 is allowable.

The Examiner rejected claims 30 and 37 under 35 U.S.C. § 102(b) as being anticipated by PCI-to-PCI Bridge Architecture Specification ("PCI-to-PCI Bridge"). In order to clearly distinguish claims 30 and 37 from the cited prior art, the Applicant has amended claim 30 and 37 to expressly require that the claimed switch be a HyperTransport ("HT") switch. Thus, none of the prior art cited by the Examiner, alone or in any combination, performs the method claimed in amended claims 30 or 37. As a result, Applicant believes that independent claims 30 and 37, together with dependent claims 31 – 36 and 38 – 43, are allowable.

The Examiner rejected claim 44 under 35 U.S.C. § 102(b) as being anticipated by PCI-to-PCI Bridge Architecture Specification ("PCI-to-PCI Bridge"). In order to clearly distinguish claim 44 from the cited prior art, the Applicant has amended claim 44 to expressly require that the claimed switch be a HyperTransport ("HT") switch. Thus, none of the prior art cited by the Examiner, alone or in any combination, performs the method claimed in amended claim 44. As a result, Applicant believes that independent claim 44, together with dependent claims 45 and 46, are allowable.

The Examiner rejected claim 48 under 35 U.S.C. § 102(b) as being anticipated by PCI-to-PCI Bridge Architecture Specification ("PCI-to-PCI Bridge"). In order to clearly distinguish claim 48 from the cited prior art, the Applicant has amended claim 48 to expressly require that the claimed switch be a HyperTransport ("HT") switch. Thus, none of the prior art cited by the Examiner, alone or in any combination, performs the method claimed in amended claim 48. As a

result, Applicant believes that independent claim 48, together with dependent claims 49 and 50, are allowable.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

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